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(54) Integrated semiconductor transistor with current sensing

(57) The present invention relates to semiconductor integrated transistors comprising a conduction section (CE,ME) and a sense section (SE) for the current flowing through the conduction section (CE,ME), both sections being located within a region (RG).

To ensure that sensing is accurate and takes into account that the surface of the power transistor reach in operation a non-uniform temperature, the conduction section (CE,ME) and sense section (SE) are located in such a manner that, in operation, their temperature distributions are substantially equal.

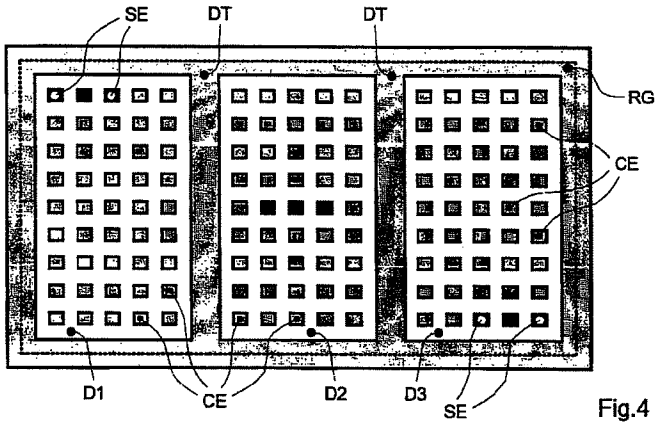

Fig.4

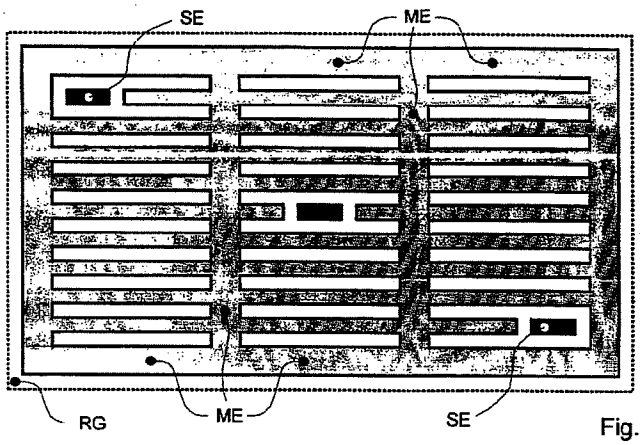

Fig.5

EP 0 892 435 A1

Description

This invention relates to a method of sensing current in a transistor, according to the preamble of Claim 1, and to semiconductor transistors of the integrated type, according to the preamble of either Claim 3 or 4, which implement the method.

Sensing a current which is flowing along the main conduction path of a transistor, i.e. the collector-emitter current for BJT transistors and the source-drain current for MOSFET transistors, is a fairly common occurrence, especially with power transistors; this can be useful to protect the transistor against overloads, or in certain applications, to control the current being delivered to the load by the transistor.

The commonest method for effecting this sensing is to connect, in series with the main conduction path of the transistor, a resistor having an exactly known very low and stable value, and then measure the voltage drop across the resistor; the voltage drop introduced by the resistor is somewhat disadvantageous for certain applications; in addition, the resistor dissipates a certain amount of electric power.

To overcome such drawbacks, another method has long been in use for semiconductor transistors of the integrated type, which consists of fabricating two transistors on the same chip, namely: a conduction one, indicated as PT in Figure 1, and a sense one, indicated as PS in Figure 1, which transistors differ from each other by their conduction areas; if their control voltages, VGS in the instance of the MOSFET transistors in Figure 1, are made identical, then the ratio of the currents flowing through them will be equal to the ratio of their conduction areas.

As is well known, power transistors of the integrated type are often formed by a plurality of identical elements, usually known as "cells"; Figure 2B shows a cross-section of an exemplary cell for MOSFET transistors, and Figure 3 is a schematic top view of a power transistor PW comprising a plurality of such cells located within a region RG of the chip, in this example an array of 12 columns and 9 rows.

The cell of Figure 2B is formed within an epitaxial layer EPI of the N- type, overlying a substrate SUB of the P type, which layer constitutes the drain terminal DT; the cell is formed by a bulk well BD of the P type wherein two source wells SD of the N+ type are provided; the wells RD and SD are surface contacted together by a metal structure forming the source terminal ST; located at the surface included between the edges of the wells SD and the edge of the well BD are two polysilicon structures which form the control terminal GT and are isolated from the surface by an insulating material. When looked from the top, the cell appears as a closed, e.g. circular, area corresponding to the well BD and wherein is a girdle, e.g. a circular one, corresponding to the wells SD.

The cells forming the power transistor PW are divided into two sections: the conduction elements CE which are connected together in parallel and form the conduction transistor PT, i.e. the conduction section of the power transistor PW, and the sense elements SE which are connected together in parallel and form the sense transistor PS, i.e. the sense section of the power transistor PW.

As shown in Figure 3, a set of, 8 in the example, elements next to each other are usually selected for the sense elements SE; in this way, the necessary connections become easier to make. In the example of Figure 3, the ratio of the conduction areas is 8/100; in practical applications, this ratio is generally much lower, e.g. 8/8000=1/1000.

By this method, definitely better sensing results are obtained than those to be obtained with the resistor, and with none of its disadvantages; by first approximation no sensing errors occur; of course, the area occupied by the transistor on the chip is slightly larger.

However, it has been found by second approximation analysis that the current sensed by the sense transistor PS is not exactly proportional to that flowing through the conduction transistor PT. This discrepancy has been attributed to the fact that, in electric operation, the region RG occupied by the power transistor has a temperature which varies according to position; for example, the middle zone may be at 70°C and, at the same time, the peripheral zones be at 50°C. Furthermore, each of the conduction and sense elements is affected by its instant temperature, so that the current through them will be different for the same control voltage.

It is the object of this invention to provide a method of sensing a current of a transistor, which is more accurate than conventional ones, and to provide transistors for its implementation.

This object is achieved by a method having the features of Claim 1, and transistors having the features of Claim 3 or 4; further advantageous aspects of this invention are set forth in the subclaims.

The idea behind this invention is to have the conduction and sense sections located in such a manner that, in operation of the transistor, they will have substantially identical temperature distributions, their operation and behavior will be substantially equal and the resulting sensing can be highly accurate.

The invention can be better understood from the following description, to be read in conjunction with the accompanying drawings, in which:

Figure 1 is a circuit diagram of a conventional system for sensing and controlling a current in a MOSFET power transistor;

Figure 2A is a sectional view through a first conventional MOSFET power transistor cell;

Figure 2B is a sectional view through a second con-

ventional MOSFET power transistor cell;

Figure 3 is a schematic top view of a conventional "cellular" power transistor;

Figure 4 is a schematic top view of a "cellular" power transistor according to the invention; and

Figure 5 is a schematic top view of a "mesh" power transistor according to the invention.

Shown in Figure 1 is a circuit diagram of a conventional system for sensing and controlling a current in a MOSFET power transistor PW.

The transistor PW comprises a proper conduction section corresponding to a conduction transistor PT, and a sense section corresponding to a sense transistor PS.

The transistors PT and PS have drain terminals connected together and to a supply voltage reference VCC, and control terminals jointly connected to the output of an operational amplifier OP. The source terminal of the transistor PT is connected to a load LD referred to a ground GND. The source terminal of the transistor PS is connected to a controlled current generator IG, also referred to the ground GND; the generator IG has a control terminal CNT whereby the value of the current therethrough can be determined. The source terminals of the transistors PS and PT are connected to the inverting and non-inverting inputs, respectively, of the operational amplifier OP.

Because of the high gain of the operational amplifier OP, the potentials at its inverting and non-inverting inputs will be substantially the same in operation of the system; accordingly, the transistors PS and PT will have substantially equal voltages VGS, and the ratio of the values of their respective currents will be equal to the ratio of their respective conduction areas, e.g. "k".

If the generator IG forces a current IR on the transistor PS, neglecting the current drawn by the inverting input of the amplifier OP which is quite small, a current IL flowing through the load LD will be "k" times IR, neglecting the current drawn by the non-inverting of the amplifier OP which is also quite small.

In operation of the a system as shown in Figure 1, the region RG of the chip occupied by the transistor PW will rise in temperature. It has been determined, from actual measurements and simulations, that the curve of temperature versus position has a shape resembling that of a Gaussian function, when a narrow horizontal or vertical portion of this region is taken; as the length of the portion, i.e. one dimension of the region RG, is increased, the curve changes to become substantially flat at the middle, while retaining its Gaussian shape at the ends. When the region RG is divided into small square or rectangular portions having, for example, the same dimensions as the transistor cells (lateral length and diameter in the 10-micron range), and assuming the temperature to be uniform inside these portions, the statistical distribution of temperature will have a pattern which depends on: the electrical and environmental operation conditions of the transistor; the shape, size and layout of the cells within the region RG; as well as on similar parameters relating to whatever may be around the region RG on the chip. For example, it could be found that 50% of the region RG is at a temperature in the range of 65° to 75°C, 30% in the 55° to 65°C range, and 20% in the 45° to 55°C range.

The method of this invention for sensing the current in a semiconductor transistor of the integrated type applies to transistors which comprise a conduction section located within a region of the chip, and a sense section for the current flowing through the conduction section, and provides for the sense section to be located inside that region, but such that, in operation of the transistor, its temperature distribution is substantially the same as the temperature distribution of the conduction section.

Thus, the environmental conditions of the two sections will be substantially identical; this being prerequisite for a highly accurate sensing, regardless of the mode of operating the sense section.

Of course, for high accuracy sensing, the sense section should be implemented by integrated structures similar to those forming the conduction section.

In this way, not only their environmental conditions but also their operation and performance will be the same.

There are basically two ways to the fabrication of power transistors: a "cellular" construction as described, for example, in Patent Application EP 252 236, and a "mesh" construction as described, for example, in Patent Applications EP 772 242 and EP 782 201; the method of this invention applies to both constructions.

Referring to Figure 4, the semiconductor integrated transistor of the "cellular" type, according to this invention, comprises:

a) a conduction section formed by a first plurality of conduction elements CE located within a region RG and connected in parallel together; and

b) a sense section for the current flowing through the conduction section which is formed by a second plurality of sense elements SE, similar to the conduction elements CE and being located within the region RG and connected in parallel together;
the position of the elements CE, SE being such that, in operation of the transistor, the temperature distribution of the conduction elements CE is substantially equal to the temperature distribution of the sense elements SE.

The cell used for the transistor of Figure 4 has the cross-section shown in Figure 2A. It is fabricated within

an epitaxial layer EPI of the N- type, overlying a substrate SUB of the P type; the cell is formed by a bulk well BD of the P type containing two source wells SD of the N+ type; the wells BD and SD are surface contacted to each other by a metal structure which forms the source terminal ST; two polysilicon structures, forming the control terminal GT and being isolated from the surface by an insulating material, are provided at the surface between the edges of the wells SD and the edge of the well BD.

A buried layer BL of the N+ type is provided between the substrate SUB and the layer EPI, at the cell location; the layer BL is surface contacted by means of metal structures that form the drain terminal DT, through sinker wells of the N+ type.

Looking from the top, the cell appears as a closed, e.g. square, area corresponding to the well BD, on whose inside is a, e.g. square, girdle corresponding to the wells SD.

The layer BL is generally a single layer shared by several cells. In the example of Figure 4, the layer BL is shared by all the cells CE, SE of the transistor, and underlies them across the whole region RG; in order to reduce the resistance of this layer, the well SK and the drain metal structure DT are provided in the form of three rectangular girdles joining one another and defining three subregions D1, D2, D3.

The provision of a well SK and structure DT within the region RG may affect the temperature distribution somewhat.

Referring to Figure 5, the semiconductor integrated transistor of the "mesh" type, according to this invention, comprises:

a) a conduction section formed by at least one conduction mesh ME located inside a region RG; and

b) a sense section for the current flowing through the conduction section which is formed by a plurality of sense elements SE, structurally similar to the conduction mesh ME and being located within the region RG and connected in parallel together;
the position of the sense elements SE being such that, in operation of the transistor, the temperature distribution of the conduction mesh(es) ME is substantially equal to the temperature distribution of the sense elements SE.

The mesh ME of the transistor in Figure 5 can be split up into three substantially equal parts joined to one another; each part is formed of a rectangular girdle having a given thickness and its internal area crossed by a plurality of thinner parallel strips which are joined at the girdle. The transistor of Figure 5 could also be thought of as having three conduction meshes which are joined together at three contiguous subregions, respectively.

The cross-section of a strip may be similar to that of a cell. The strip used for the transistor of Figure 5 has the cross-section shown in Figure 2B. This is formed within an epitaxial layer EPI of the N- type, over a substrate SUB of the P type defining the drain terminal DT; the strip is formed of a bulk well BD of the P type containing two source wells SD of the N+ type; the wells BD and SD are surface contacted together by a metal structure which forms the source terminal ST; provided at the surface between the edges of the well SD and the edge of the well BD are two polysilicon structures forming the control terminal GT and being isolated from the surface by an insulating material.

The well BD corresponds essentially to the mesh ME, and accordingly, has the same shape; the wells SD are usually present in the strips only. The sense elements SE are obtained by so interrupting the strips, and hence the well BD, as to form isolated wells from the mesh ME; inside these isolated wells, the wells SD are laid such that they are out of all contact with the layer EPI.

Of course, the shape and structure of the mesh will affect the temperature distribution.

The following considerations basically apply to either types of power transistors.

Where the region RG has a substantially rectangular shape, the sense elements SE can be laid substantially along at least one of the rectangle diagonals; in this way, a sense element can be placed at the hottest spot, the center of the rectangle, and at the coldest spot, i.e. the edge of the rectangle.

For the sake of design simplicity, the sense elements SE can be laid out in a substantially uniform manner along the diagonal line; this usually would not meet exactly the condition for equality of the temperature distributions.

As previously mentioned, particularly in relation to Figure 4, the region RG may be divided into non-contiguous subregions D1, D2, D3.

In this case, it matters to have at least one sense element located within each subregion.

Where the subregions are laid contiguously, this division has a fairly limited effect on temperature distribution.

Should the non-contiguous layout of the subregions significantly affect the distribution of temperature, then a plurality of sense elements SE are better provided in each subregion, and their positions should be such that, in operation of the transistor, their temperature distribution is substantially the same as the temperature distribution of the corresponding subregion.

As the skilled persons in the art will readily recognize, this invention can also find an application to BJT power transistors, even though it has been described in connection with MOSFET power transistors; in fact, BJT power transistors also admit of "cellular" and "mesh" constructions and have a control voltage, the voltage VBE.

Such MOSFET and BJT power transistors can either be sold as discrete components or included within

more complex integrated circuits which also accommodate, for example, driving circuitry for the power transistor.

Claims

1. A method for sensing current in a semiconductor transistor of the integrated type having a conduction section (CE,ME) located within a region (RG) and a sense section (SE) for the current flowing through said conduction section (CE,ME), characterized in that said sense section (SE) is located within said region (RG) in such a manner that, in operation of the transistor, its temperature distribution is substantially equal to the temperature distribution of the conduction section (CE,ME).

2. A method according to Claim 1, wherein said sense section (SE) is formed of integrated structures similar to those forming said conduction section (CE,ME).

3. A semiconductor integrated transistor, comprising:

   a) a conduction section formed by a first plurality of conduction elements (CE) located within a region (RG) and connected in parallel together; and

   b) a sense section for the current flowing through said conduction section which is formed by a plurality of sense elements (SE), similar to the conduction elements (CE), and located within said region (RG) and connected in parallel together;
   characterized in that the position of said elements (CE,SE) is such that, in operation of the transistor, the temperature distribution of the conduction elements (CE) is substantially equal to the temperature distribution of the sense elements (SE).

4. A semiconductor integrated transistor, comprising:

   a) a conduction section formed by at least one conduction mesh (ME) located within a region (RG); and
   b) a sense section for the current flowing through said conduction section which is formed by a plurality of sense elements (SE), structurally similar to said conduction mesh (ME), and located within said region (RG) and connected in parallel together;
   characterized in that the position of said sense elements (SE) is such that, in operation of the transistor, the temperature distribution of the conduction mesh or meshes (ME) is substantially equal to the temperature distribution of the sense elements (SE).

5. A transistor according to either Claim 3 or 4, wherein said region (RG) is substantially rectangular in shape and said sense elements (SE) are located substantially along at least one of the diagonal lines of the rectangle.

6. A transistor according to Claim 5, wherein said sense elements (SE) are located substantially uniformly along the diagonal or diagonals.

7. A transistor according to either Claim 3 or 4 or 5, wherein said region (RG) is divided into non-contiguous subregions (D1,D2,D3).

8. A transistor according to Claim 7, wherein each subregion (D1,D2,D3) contains at least one of said sense elements (SE).

9. A transistor according to Claim 8, wherein each subregion (D1,D2,D3) contains a plurality of said sense elements (SE), and their position is such that, in operation of the transistor, their temperature distribution is substantially equal to the temperature distribution of the corresponding subregion.

10. An integrated circuit incorporating at least one transistor as claimed in Claim 3 or Claim 4.

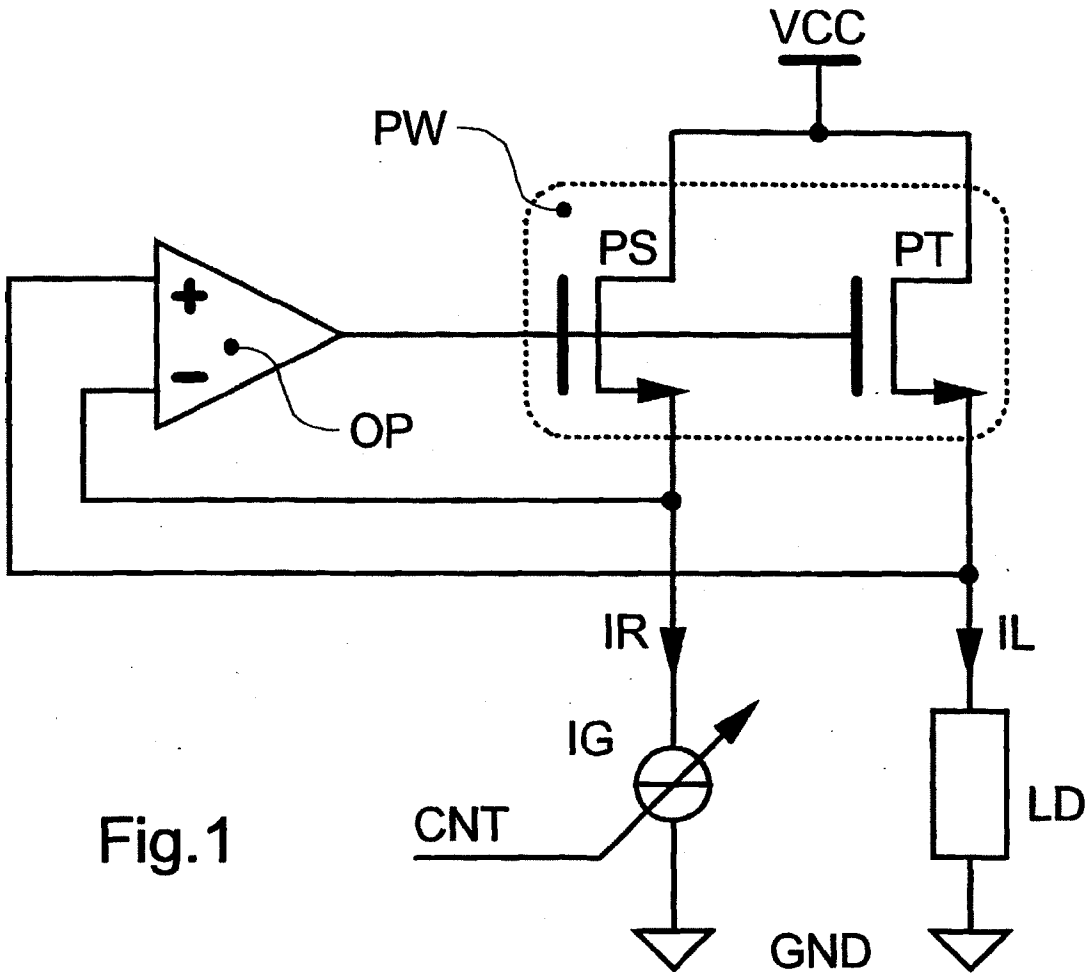

Fig.1

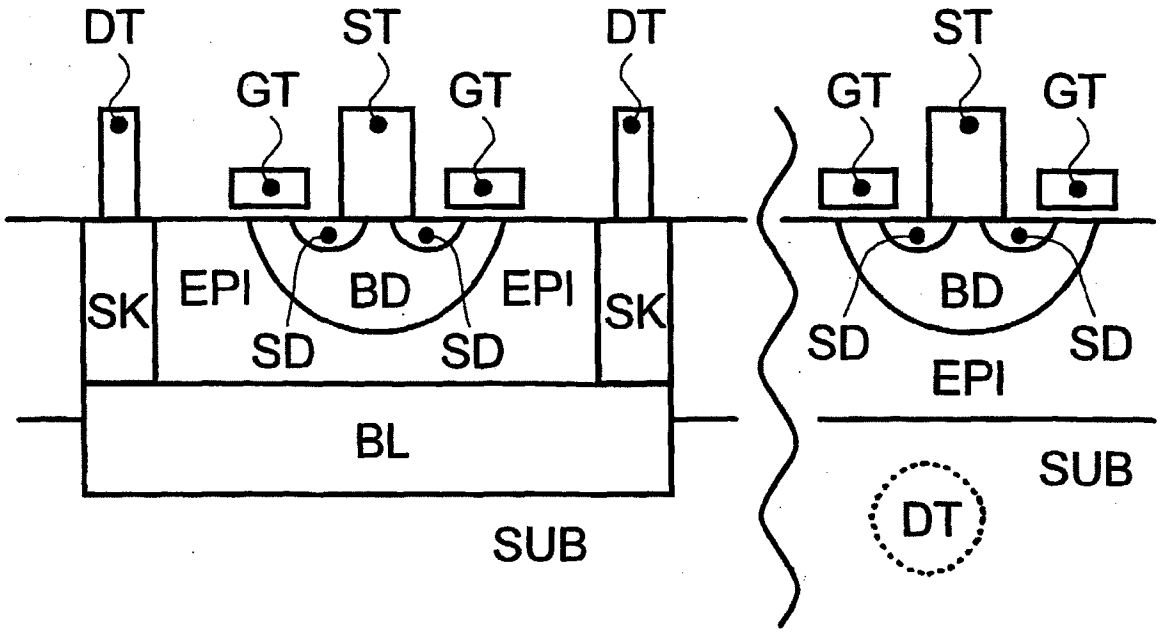

Fig.2A

Fig.2B

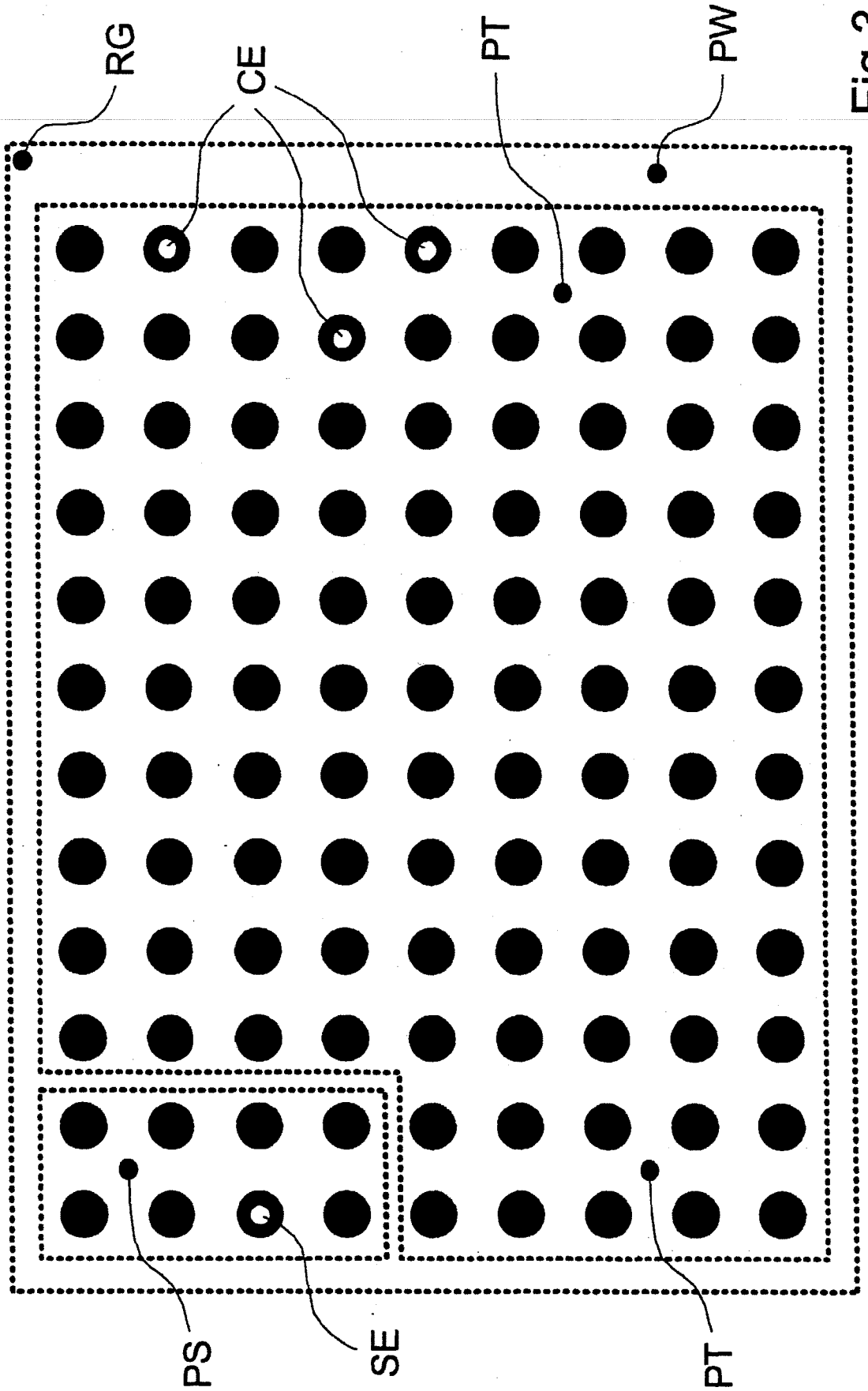

Fig.3

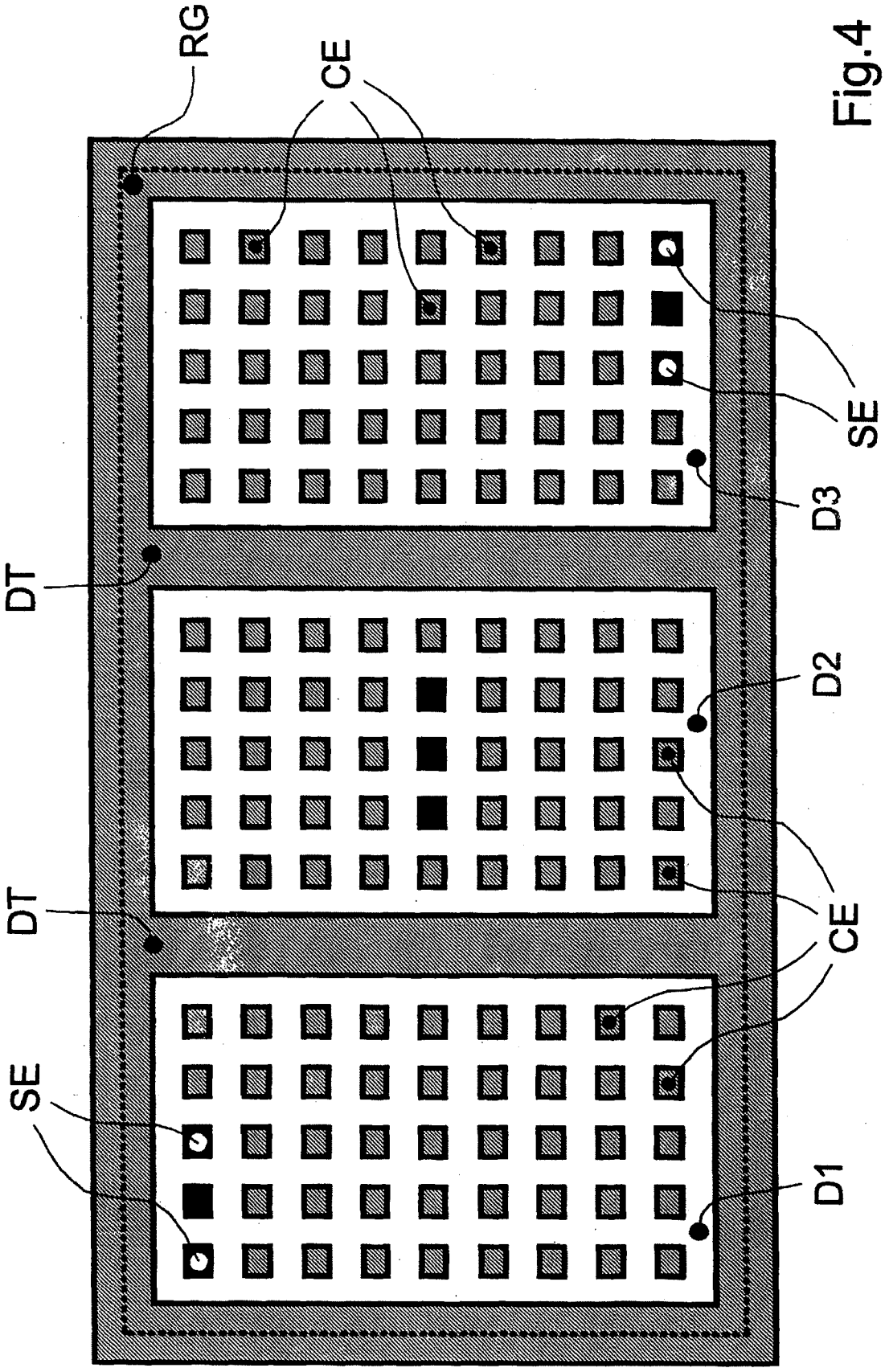

Fig.4

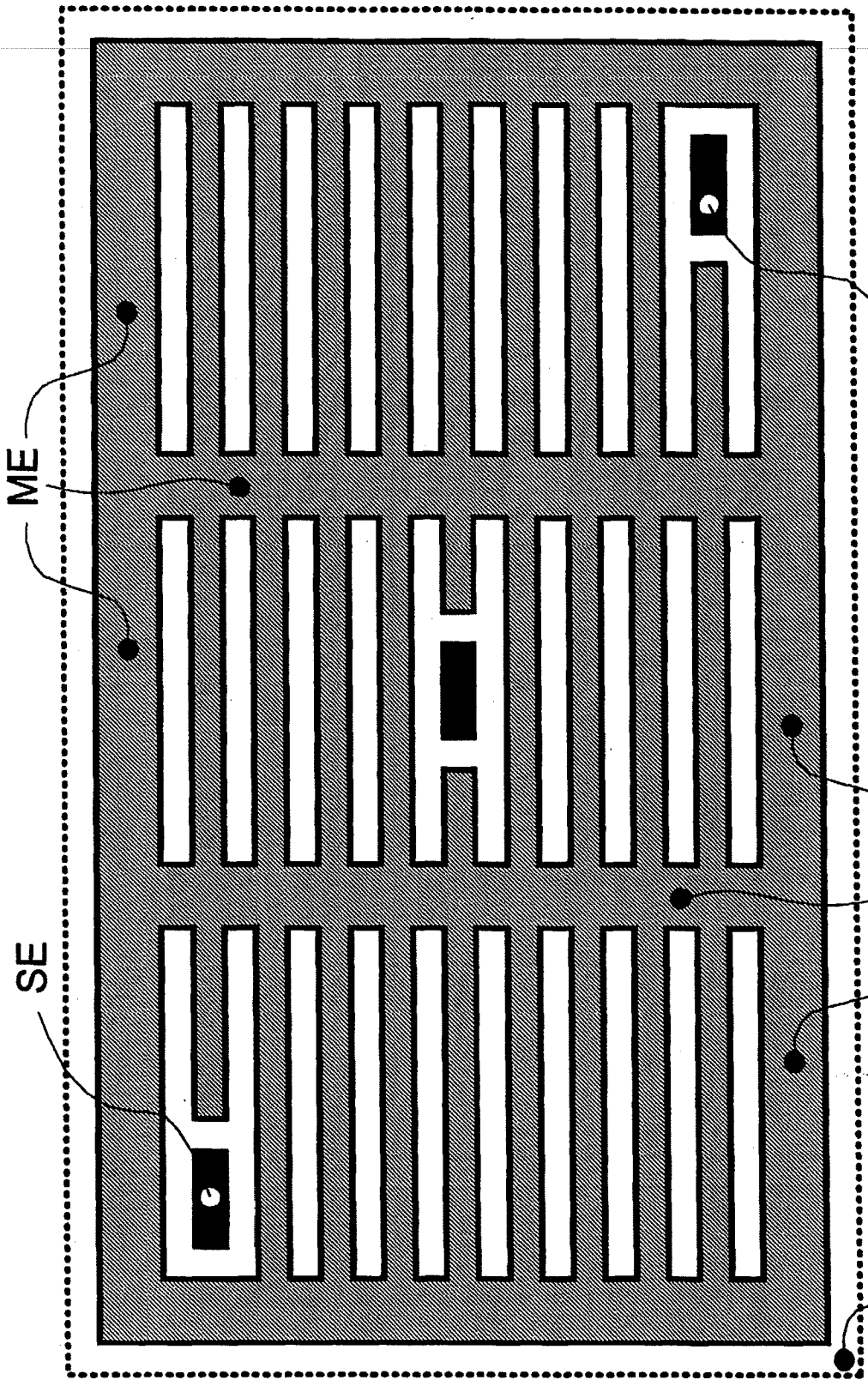

Fig.5

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EUROPEAN SEARCH REPORT

Application Number
EP 97 83 0347

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 649 176 A (FUJI ELECTRIC CO LTD) * abstract; figures *	1-10	H01L27/02
A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 504 (E-1430), 10 September 1993 & JP 05 129604 A (TOSHIBA CORP), 25 May 1993, * abstract *	1-10	
A	PATENT ABSTRACTS OF JAPAN vol. 008, no. 139 (E-253), 28 June 1984 & JP 59 047763 A (HITACHI SEISAKUSHO KK), 17 March 1984, * abstract *	1-10	
A	US 5 543 632 A (ASHLEY DONALD J) * abstract *	1-10	
A	EP 0 670 600 A (FUJI ELECTRIC CO LTD) * column 2, line 39 - line 47 * * column 3, line 6 - line 31; figures *	1-10	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	US 5 365 085 A (TOKURA NORIHITO ET AL) * column 2, line 45 - column 3, line 6 *	1-10	
A	EP 0 132 861 A (PHILIPS NV) * page 5, line 24 - line 27 *	1-10	
D,A	EP 0 252 236 A (TOKYO SHIBAURA ELECTRIC CO) * claims *	3	
D,A	EP 0 772 242 A (SGS THOMSON MICROELECTRONICS ;CONS RIC MICROELETTRONICA (IT)) * abstract *	4	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 November 1997	Vendange, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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EUROPEAN SEARCH REPORT

Application Number
EP 97 83 0347

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	EP 0 782 201 A (SGS THOMSON MICROELECTRONICS ;CONS RIC MICROELETTRONICA (IT)) * abstract *	4	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

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